THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 39

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte CAROL E. BASSETT,
ROBERT G. CAMPBELL,
MARILYN J. LANG and SRIDHAR BEGUR

_____

Appeal No. 95-4957
Application 07/950,979[1]

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ON BRIEF

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Before THOMAS, JERRY SMITH and CARMICHAEL, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed September 23, 1992. According to appellants, the application is a continuation of Application 07/472,064, filed January 31, 1990, now abandoned.

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-6, 8, 10-19, 22, 24, 26-29, 34 and 35, which constituted all the claims remaining in the application. An amendment after final rejection was filed on September 26, 1994 and was entered by the examiner. This amendment cancelled claim 26 so that it is not part of this appeal.

The claimed invention pertains to an apparatus and method for retrieving data from a system memory during a burst mode of operation of a microcomputer.

Representative claim 1 is reproduced as follows:

1. A microcomputing system comprising:

a host bus;

a microprocessor, coupled to the host bus, the microprocessor having a burst mode in which the microprocessor engages in high speed consecutive data transfers;

a system memory, coupled to the host bus, the system memory being in electrical communication with said microprocessor through the host bus, the system memory including a plurality of system memory data busses coupled to a plurality of bidirectional latching transceivers, each system memory data bus being directly coupled to the host bus through an associated bidirectional latching transceiver from the plurality of bidirectional latching transceivers; and

system memory controller means, coupled to the host bus and to the system memory, for generating control signals and for generating second addresses corresponding to data storage locations to be accessed in the system memory during the burst mode after receipt of a first host address from the

microprocessor, wherein data is obtained from the system memory at the data storage locations accessed by the second addresses and a data storage location accessed by the first host address and wherein the control signals include latching control signals which control latching of the plurality of bidirectional latching transceivers whereby data is latched from the plurality of system memory data busses directly to the host bus.

The examiner relies on the following reference:

Kronstadt et al. (Kronstadt) 4,725,945 Feb. 16, 1988

In the final rejection, some of the pending claims were rejected under 35 U.S.C. § 102(b), and the remaining claims were rejected under 35 U.S.C. § 103. In the examiner's answer, the examiner withdrew the rejection of the claims under Section 102, and the examiner indicated that all the pending claims were now rejected on a single basis under Section 103. Consequently, claims 1-6, 8, 10-19, 22, 24, 27-29, 34 and 35 now stand rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers Kronstadt taken alone.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answers for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the

rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answers.

It is our view, after consideration of the record before us, that the collective evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-6, 8, 10-19, 22, 24, 27-29, 34 and 35. Accordingly, we reverse.

In terms of the grouping of claims, appellants have only presented arguments with respect to the three independent claims 1, 13 and 34. Therefore, we will consider each of the independent claims separately for patentability. The dependent claims will stand or fall with the independent claim from which they respectively depend. See In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837

F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art

or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

As indicated by the cases just cited, the examiner has at least two responsibilities in setting forth a rejection under 35 U.S.C. § 103. First, the examiner must identify all the differences between the claimed invention and the teachings of the prior art. Second, the examiner must explain why the identified differences would have resulted from an obvious modification of the prior art.

With respect to independent claim 1, the examiner has read the claim on Kronstadt, and has concluded that the only difference between claim 1 and Kronstadt is that Kronstadt does not specifically teach using bidirectional latching transceivers [answer, page 7]. The examiner asserts that the bidirectional buffers of Kronstadt are well known equivalents of bidirectional latching transceivers, and the examiner maintains that the substitution of one for the other would have been obvious to the artisan. Appellants argue that there are several other differences between claim 1 and Kronstadt which have been ignored by the examiner. We will consider each of these alleged differences in turn and the arguments of the examiner in support of the conclusion of obviousness.

The first difference between claim 1 and Kronstadt argued by appellants is the claimed plurality of system memory data busses. According to appellants, Kronstadt discloses a memory with only a single data bus [reply brief, page 3]. The examiner argues that system busses are not typically the connections to the memory chips, and the claimed recitation would be an inherent property in Kronstadt in any case [supplemental answer, page 8]. The examiner also asserts that the claimed plurality of system memory data busses is functionally equivalent to the system data bus of Kronstadt [supplemental answer, page 9]. We agree with appellants on this point.

The busses of claim 1 are not recited simply as system busses, but rather, as system memory data busses. Thus, the busses of claim 1 must be distinguished from busses used for address or control information. The data in appellants' FIG. 3 is latched from a plurality of data busses [busses 342, 344, 346 and 348]. The data in Kronstadt is shown as being sent on a single data bus and it is the address information which routes this single bus of data. There is simply no suggestion in Kronstadt that the system memory includes a plurality of system data busses, and the examiner's contention that this feature is inherently present in Kronstadt is not only unsupported by the

record in this case but appears to be an erroneous finding as well. The only plural data busses in Kronstadt are those busses between the memory banks 16 and the d-cache 24. These busses, however, would not be considered system data busses as used in the claim because they are internal to the external memory. Additionally, whether the single data bus of Kronstadt functions equivalently to the claimed plurality of system data busses is not a valid basis per se to assert obviousness. Thus, the examiner's finding that Kronstadt teaches the claimed plurality of system memory data busses is not supported by the record in this case.

Appellants also argue that Kronstadt does not teach the claimed plurality of bidirectional latching transceivers as recited in claim 1. According to appellants, Kronstadt teaches only a single latch [26] as shown in FIG. 4. The examiner argues that the latch of Kronstadt is "equivalent to the connectivity of element 32 [sic] of Figure 3 of the present invention" [supplemental answer, page 10]. The examiner also asserts that individually associated latches would be inherently present in Kronstadt. We agree with appellants for basically the same

reasons discussed above with respect to the plurality of data busses.

Although we can agree with the examiner that the artisan would have recognized the obviousness of using bidirectional transceivers in place of bidirectional buffers, we cannot agree with the examiner that Kronstadt in any way suggests using a plurality of buffers or tranceivers for the latching of data. As noted above, Kronstadt shows only a single data line feeding either latch 26 of FIG. 4 or buffers 32 of FIG. 5. There is no support for the examiner's assertion that the claimed plurality of bidirectional latching transceivers is inherently suggested by the teachings of Kronstadt.

Appellants argue that Kronstadt does not teach a system memory controller which generates addresses in the manner recited in claim 1 [reply brief, page 4]. The examiner argues that Kronstadt teaches a system memory controller 18 as shown in FIGS. 1, 3 and 4. With respect to the specific addressing arrangement recited in claim 1, the examiner maintains that the pipelining operation of Kronstadt meets the addressing arrangement of claim 1. In our view, although Kronstadt does broadly teach a system memory controller, there is no suggestion in Kronstadt for the functions performed by this element as recited in claim 1.

We are unable to follow the examiner's reasoning that the addressing scheme of claim 1 is necessarily met by the pipeline processing of Kronstadt. The examiner has found equivalence between the burst mode transfer of data and the pipelining of Kronstadt [supplemental answer, page 8]. We see no reason why the memory controller of Kronstadt would have to generate any addresses in addition to those received from the host processor in pipelined fashion. In fact, the generation of "REAL ADDRESS" between the CPU 10 and the memory controller 18 of Kronstadt would suggest that the memory controller does not generate additional addresses. There is no evidence in the record of this case that any generation of second addresses is required in the operation of the Kronstadt memory.

In summary, there are several differences between the recitations of claim 1 and the teachings of Kronstadt which have been asserted by appellants as patentably distinguishing over the reference. The examiner has basically dismissed all these differences as being inherent, equivalent or simply obvious. The record does not support the examiner's findings. Therefore, we

find appellants' arguments more persuasive than the examiner's arguments. Although there is a certain similarity between the elements named in Kronstadt and the elements of claim 1, the examiner has not addressed all the limitations recited in the claim. Accordingly, we do not sustain the rejection of claim 1 as unpatentable over the teachings of Kronstadt. Since claims 2-6, 8 and 10-12 depend from claim 1, we also do not sustain the rejection of these claims.

Although appellants have argued independent claims 13 and 34 separately, we note that claims 13 and 34 contain the same limitations discussed above with respect to claim 1 and that the examiner lumped these claims with claim 1 in explaining the rejection. Since the exact same issues are presented for resolution with respect to claims 13 and 34, we do not sustain the rejection of these claims for the same reasons discussed above.

Since claims 14-19, 22, 24, 27-29 and 35 depend from one of these claims, we also do not sustain the rejection of these claims.

In summary, we have not sustained the examiner's rejection of any of the claims on appeal before us. Therefore,

the decision of the examiner rejecting claims 1-6, 8, 10-19, 22, 24, 27-29, 34 and 35 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT)) APPEALS AND)) INTERFERENCES
JAMES T. CARMICHAEL Administrative Patent Judge	)

Records Manager
Legal Department, 20B0
Hewlett-Packard Company
P.O. Box 10301
Palo Alto, CA 94303-0890